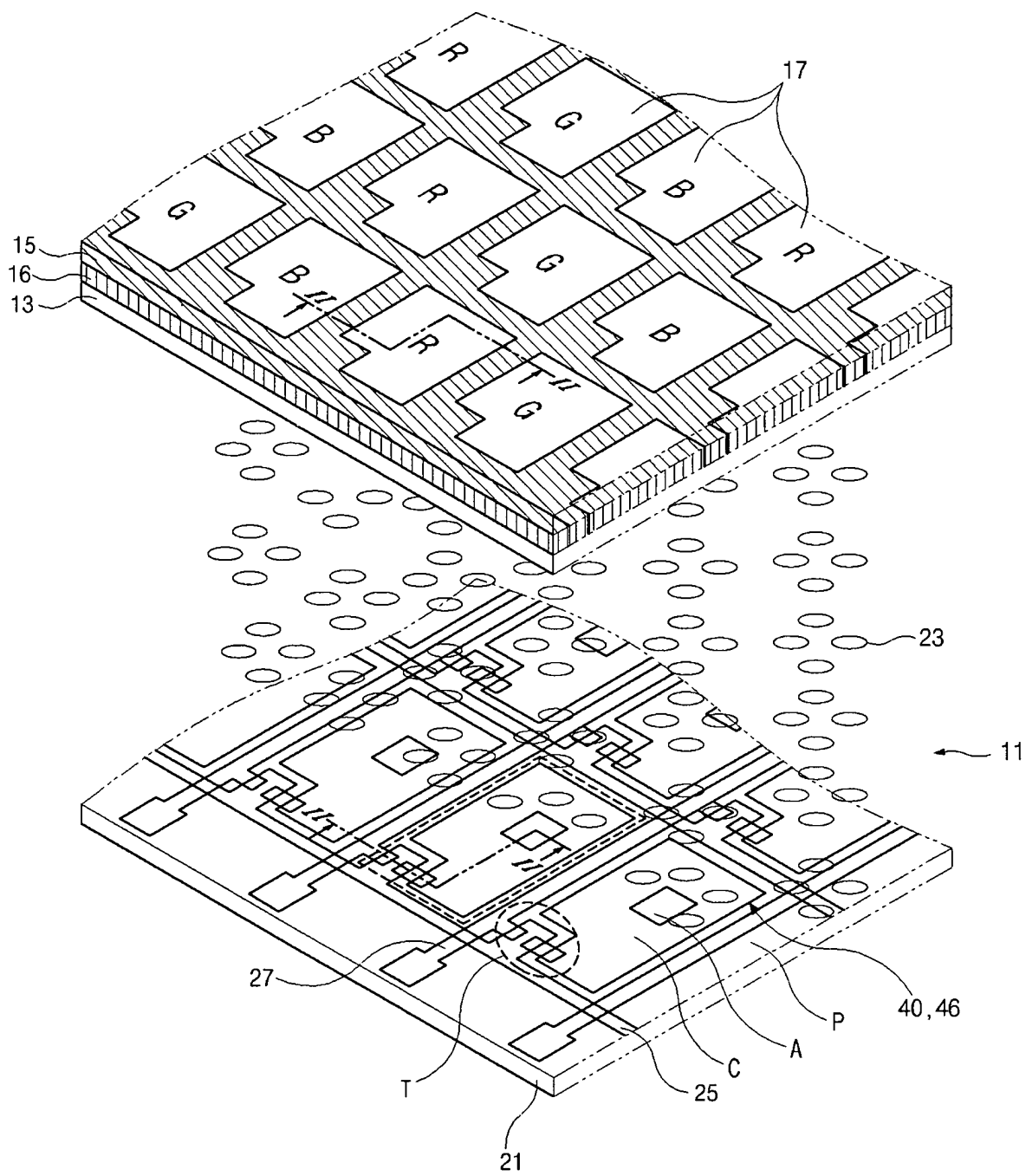


FIG. 1
RELATED ART



This cross-sectional view shows a multi-layered structure. The top layer is labeled 17, with sub-regions 17a, 17b, and 17c. Below this is a layer labeled 15. A layer labeled 16 is positioned below 15, with features G and R. A layer labeled 13 is below 16. A layer labeled 23 is below 13. A layer labeled 42 is below 23, with features 34, 36, 32, 30, 46, 40, and 27. A layer labeled 38 is below 42. A layer labeled 10 is below 38. A layer labeled 21 is below 10. A layer labeled 8 is below 21. Dimensions T, C, A, C, P1, P2, and E are indicated at the bottom. The structure is bounded by vertical lines II on the left and right.

FIG. 3
RELATED ART

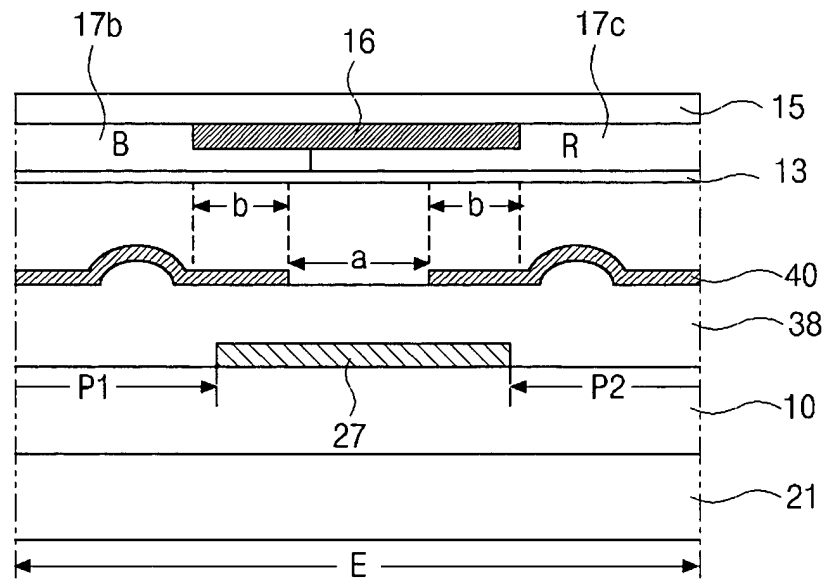


FIG. 4

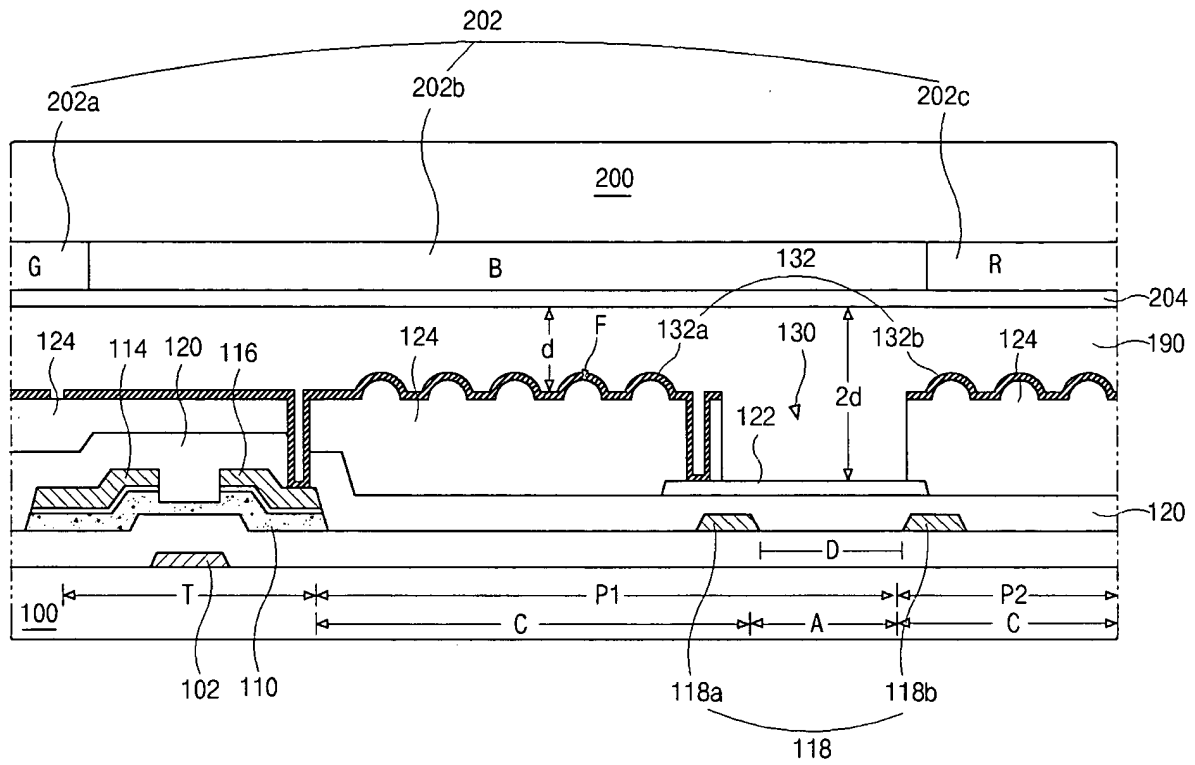


FIG. 1 is a plan view of a semiconductor device 100. The device includes two identical circuit blocks separated by a central region 106. Each block contains a transistor 102 with a gate 114 and a drain 116, and a diode 110 with an anode 126 and a cathode 128. The blocks are defined by regions 132 and 122. Dimensions P1, P2, C, and A are indicated. VI and T are also labeled.

FIG. 6A

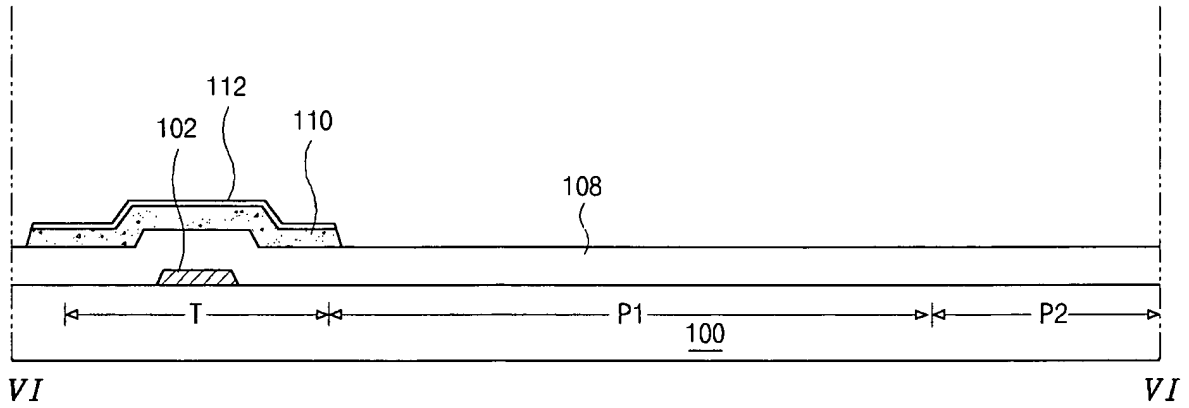


FIG. 6B

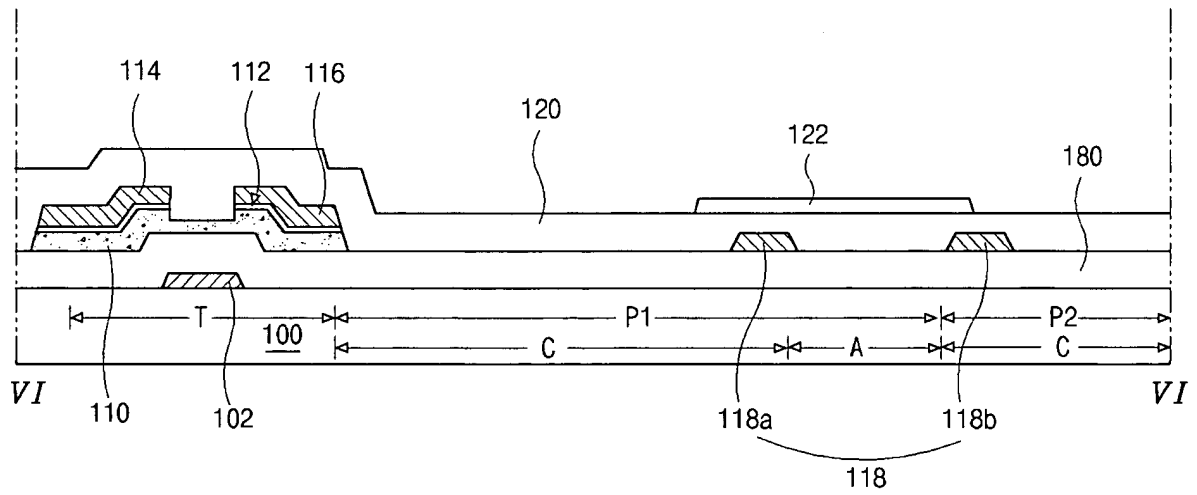


FIG. 6C

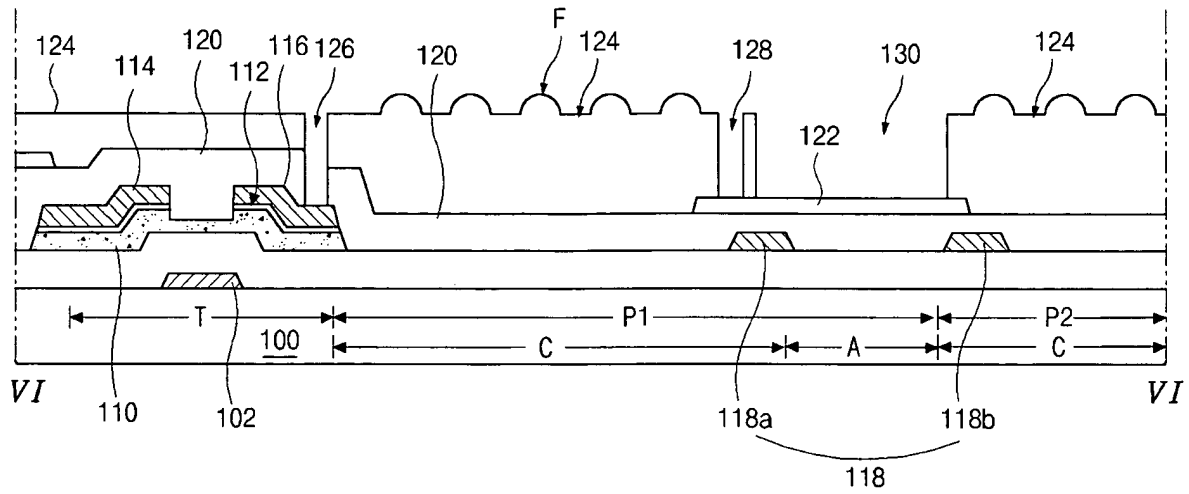


FIG. 6D

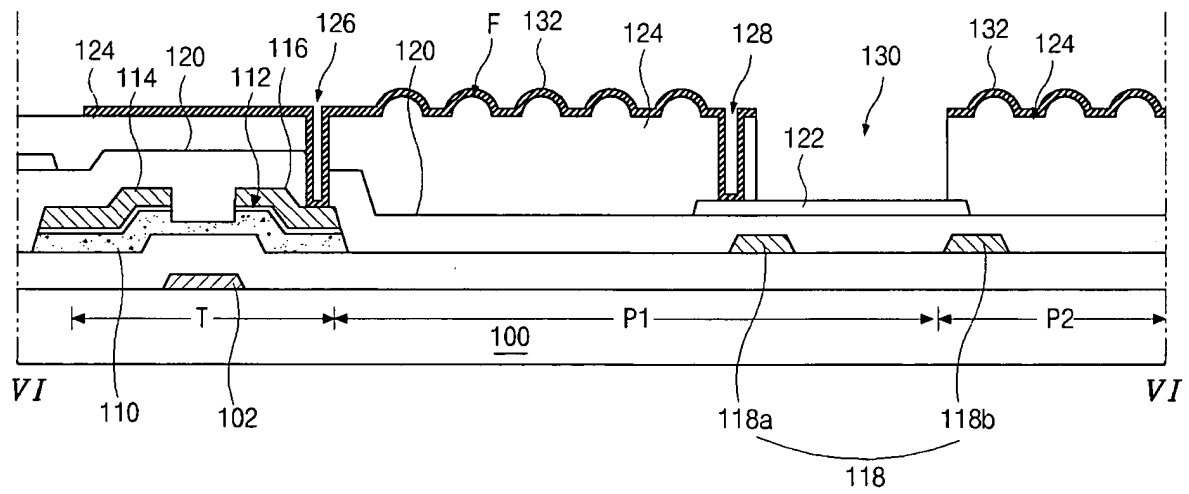


FIG. 7

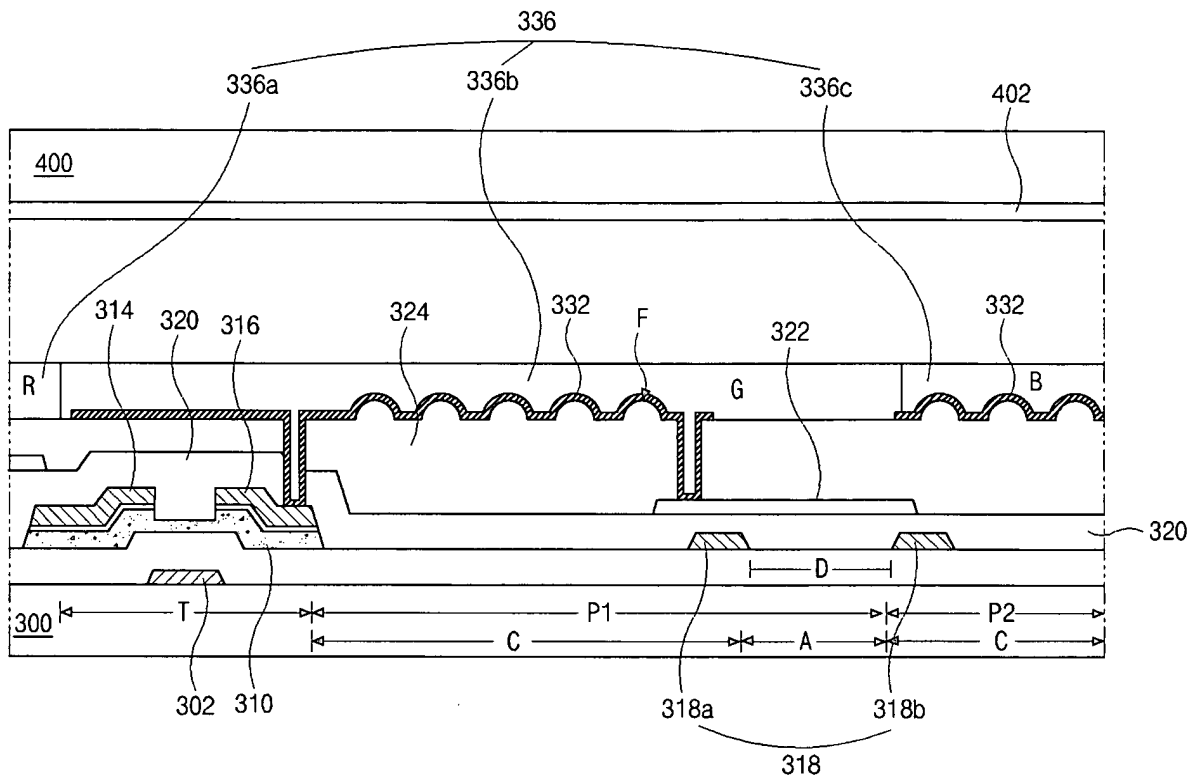


FIG. 8

